REMARKS

This is a full and timely response to the final Office Action of September 25, 2007. Reexamination, reconsideration, and allowance of the application and all presently pending claims are respectfully requested.

Upon entry of this Second Response, claims 1, 3-8, 12-14, 16, 17, and 21-31 are pending in this application. Claims 3, 22, 27, and 30 are directly amended herein. It is believed that the foregoing amendments add no new matter to the present application.

In addition, it is believed that the amendments address claim objections and issues under 35 U.S.C. §112 raised for the first time in the outstanding Office Action. Applicants have not been afforded a previous opportunity to respond to such claim objections and issues under 35 U.S.C. §112, and it is believed that the amendments will not require a new search by the Examiner. Accordingly, Applicants respectfully request that the amendments be entered pursuant to 37 C.F.R. §1.116.

Response to Drawing Objection

The outstanding Office Action indicates that the drawings are objected to as allegedly failing to show every feature specified by claim 27. Applicants submit that claim 27 has been amended herein to recite "wherein the logic is configured to refrain from purging the instruction queue in response in response to the purge signal ***unless*** at least one of the translation pairs stored in the TLB corresponds to the purge signal." (Emphasis added). It is believed that such features are shown at least by Figure 5 of the instant disclosure. Accordingly, Applicants respectfully request that the objection to the drawings be withdrawn.

Response to Claim Objections

Claims 3 and 5 presently stand objected to for referring to a previously canceled claim. Claims 3 and 5 have been amended herein thereby mooting the objections to these claims. Accordingly, Applicants respectfully request that the objections to claims 3 and 5 be withdrawn.

Response to §112 Rejection

Claim 27 presently stands rejected under 35 U.S.C. §112, first paragraph, as allegedly based on a disclosure which is not enabling. Further, claims 22 and 30 presently stand rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants submit that claims 22, 27, and 30 have been amended thereby mooting the rejections of these claims under 35 U.S.C. §112. Thus, Applicants respectfully request that the 35 U.S.C. §112,first paragraph, rejection of claim 27 and the 35 U.S.C. §112, second paragraph, rejections of claims 22 and 30 be withdrawn.

Response to §103 Rejections

In order for a claim to be properly rejected under 35 U.S.C. §103, the combined teachings of the prior art references must suggest all features of the claimed invention to one of ordinary skill in the art. See, *e.g.*, *In Re Dow Chemical Co.*, 837 F.2d 469, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 642 F.2d 413, 208 U.S.P.Q. 871, 881 (C.C.P.A. 1981).

Claim 1

Claim 1 presently stands rejected under 35 U.S.C. §103 as allegedly being unpatentable over Applicants' Admitted Prior Art ("AAPA") in view of *Moore* (U.S. Patent No. 5,437,017). Claim 1 reads as follows:

> "1. A processor purging system, comprising:
> a translation lookaside buffer (TLB) having a plurality of translation pairs;
> at least one memory cache; and
> logic configured to make a determination whether at least one of the translation pairs corresponds to a purge signal and to purge, in response to the purge signal, each of the translation pairs in the TLB corresponding to the purge signal, ***the logic further configured to transmit, based on the determination, a purge detection signal indicative of whether at least one translation pair in the TLB corresponds to the purge signal and to determine, based upon the purge detection signal, whether to search the memory cache for information to be purged based on the purge signal.***" (Emphasis added).

Applicants respectfully assert that the alleged combination fails to suggest at least the features of claim 1 highlighted above. Thus, the 35 U.S.C. §103 rejection of claim 1 should be withdrawn.

In this regard, it is candidly admitted in the Office Action that:

> "AAPA does not explicitly teach that the logic further configured to transmit, based on the determination, a purge detection signal indicative of whether at least one translation pair in the TLB corresponds to the purge signal and to determine, based upon the purge detection signal, whether to search the memory cache for a information to be purged based on the purge signal."

However, it is alleged in the Office Action that *Moore* teaches the features missing from the AAPA and that it would be obvious to combine *Moore* with the AAPA. In particular, it is alleged that:

> "Moore teaches a system and method for maintaining TLB coherency between the TLB and memory queues (i.e. instruction queue) in a multiprocessor system (abstract). Moore accomplishes this by broadcasting a TLB invalidate instruction to all processors (Fig. 4). Once all processors have indicated that the instruction has completed execution, a determination is made whether the memory queue has reached coherency (col. 9 lines 30-42).
> It would have been obvious to one of ordinary skill in the art at the time of the inventions to include transmitting a signal to indicate when to check for coherency in the memory queue as taught by Moore. One would be motivated by the desire to ensure that the TLB was purged of all invalid entries before performing a coherency check on the rest of the memory queues."

Applicants respectfully assert that, even if it is assumed for the sake of argument that the above allegations are true, the Office Action nevertheless fails to establish a *prima facie* case of obviousness, and the 35 U.S.C. §103 rejection of claim 1 is, therefore, improper for at least this reason.

In this regard, *Moore* apparently teaches that a translation lookaside buffer invalidate (TLBI) instruction is broadcast to each processor in a multiprocessor system. See Abstract and column 8, lines 37-44. If all of the processors "accept" the TLBI instruction, then each processor apparently initiates a purge of its respective translation lookaside buffer (TLB). However, if any of the processors do not accept the TLBI instruction, then none of the processors initiate execution of the TLBI instruction. In this way, coherency among the TLBs of the multiprocessor system can be maintained. See Abstract and column 8, line 45, to column 9, line 8. If all of the processors accept the TLBI instruction, then execution of pending instructions is temporarily terminated, and once it can be ensured that no pending instructions are about to execute, the TLBI instruction is executed in each processor. See Abstract and column 9, lines 9-29. Thus, the TLB for each processor is apparently purged based on the TLBI instruction. Once a processor's TLB is purged, the processor's memory queue 36 is checked to determine whether it has achieved coherency. See column 9, lines 30-41.

However, there is nothing in *Moore* to indicate that any "purge detection signal" is used in order to check the memory queue 36 for coherency. In this regard, a "purge detection signal," as recited by claim 1, is a signal that indicates "whether at least one translation pair in the TLB corresponds to the purge signal." Indeed, it appears that the memory queue 36 is checked for coherency ***regardless*** of whether any of the translation pairs in the TLB correspond to the alleged "purge signal" (see Figure 5, blocks 122 and 124), and there is nothing in *Moore* to suggest that the searching of the memory queue 36 should be affected in any way based on a determination as to whether any of the translation pairs in the TLB correspond to the "purge signal."

Accordingly, the Office Action fails to establish a *prima facie* case of obviousness with respect to at least the features of "the logic further configured to transmit, based on the determination, a purge detection signal indicative of whether at least one translation pair in the TLB corresponds to the purge signal and to determine, ***based upon the purge detection signal***, whether to search the memory cache for information to be purged based on the purge signal," as recited by claim 1. (Emphasis added).

For at least the above reasons, Applicants assert that the cited art fails to suggest each feature of claim 1. Accordingly, Applicants respectfully request that the 35 U.S.C. §103 rejection of claim 1 be withdrawn.

Claims 3-8 and 21

Claims 3, 4, and 21 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over AAPA in view of *Moore*. Further, claims 5-8 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over AAPA in and *Moore* in view of *Mathews* (U.S. Patent No. 6,560,689). Applicants submit that the pending dependent claims 3-8 and 21 contain all features of their respective independent claim 1. Since claim 1 should be allowed, as argued hereinabove, pending dependent claims 3-8 and 21 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 12

Claim 12 presently stands rejected under 35 U.S.C. §103 as allegedly being unpatentable over AAPA in view of *Moore*. Claim 12 reads as follows:

> "12. A method for purging a processor, comprising the steps of:
> detecting whether at least one of a plurality of translation pairs in a translation lookaside buffer (TLB) corresponds to a purge signal;
> if at least one of the translation pairs in the TLB corresponds to the purge signal, purging the at least one translation pair corresponding to the purge signal;
> ***transmitting, based on the detecting step, a purge detection signal indicative of whether at least one of the translation pairs in the TLB corresponds to the purge signal***; and
> ***determining whether to purge an instruction queue based on the purge detection signal***." (Emphasis added).

For at least reasons similar to those set forth above in the arguments for allowance of claim 1, Applicants respectfully assert that the cited art fails to suggest at least the features of claim 12 highlighted above. Thus, the 35 U.S.C. §103 rejection of claim 12 should be withdrawn.

Claims 13, 14, 16, 22, and 23

Claims 13 and 14 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over AAPA and *Moore* in view of *Mathews*. In addition, claims 16, 22, and 23 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over AAPA in view of *Moore*. Applicants submit that the pending dependent claims 13, 14, 16, 22, and 23 contain all features of their respective independent claim 12. Since claim 12 should be allowed, as argued hereinabove, pending dependent claims 13, 14, 16, 22, and 23 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 17

Claim 17 presently stands rejected under 35 U.S.C. §103 as allegedly being unpatentable over AAPA in view of *Moore*. Claim 17 reads as follows:

> "17. A processor purging method, comprising:
> detecting whether at least one translation pair in a plurality of translation pairs within a translation lookaside buffer (TLB) corresponds to a purge signal;
> ***transmitting, based on the detecting step, a purge detection signal indicative of whether at least one of the translation pairs corresponds to the purge signal;***
> ***determining, based upon the purge detection signal, whether to search the memory cache for information to be purged based on the purge signal;*** and
> if at least one of the translation pairs in the TLB corresponds to the purge signal, purging from the TLB the at least one translation pair corresponding to the purge signal." (Emphasis added).

For at least reasons similar to those set forth above in the arguments for allowance of claim 1, Applicants respectfully assert that the cited art fails to suggest at least the features of claim 17 highlighted above. Thus, the 35 U.S.C. §103 rejection of claim 17 should be withdrawn.

Claim 24

Claim 24 presently stands rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over AAPA in view of *Moore*. Applicants submit that the pending dependent claim 24 contains all features of its independent claim 17. Since claim 17 should be allowed, as argued hereinabove, pending dependent claim 24 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 25

Claim 25 presently stands rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over AAPA in view of *Moore*. Claim 25 reads as follows:

> "25. A processor, comprising:
> an execution unit;
> an instruction queue coupled to the execution unit;
> a translation lookaside buffer (TLB) configured to store a plurality of translation pairs, each translation pair having a respective virtual address and a respective physical address; and
> ***logic configured to receive a purge signal and to make a determination as to whether any of the translation pairs stored in the TLB correspond to the purge signal, the logic configured to purge from the TLB each translation pair corresponding to the purge signal, the logic further configured to determine, based on the determination, whether to purge the instruction queue in response to the purge signal.***" (Emphasis added).

Applicants respectfully assert that the cited art fails to suggest at least the features of claim 25 highlighted above.

As set forth above in the arguments for allowance of claim 1, *Moore* apparently teaches that the TLB for each processor in a multiprocessor system is purged based on a TLBI instruction broadcast to each processor, provided that each processor accepts the instruction. For each processor, the memory queue 36 is checked to determine whether it has achieved coherency after the processor's TLB has been purged. See column 9, lines 30-41. However, the memory queue 36 is apparently checked for coherency ***regardless*** of whether any of the translation pairs in the TLB correspond to the alleged "purge signal" (see Figure 5, blocks 122 and 124), and there is nothing in *Moore* to suggest that the searching of the memory queue 36 should be affected in any way based on a determination as to whether any of the translation pairs stored in the TLB correspond to the "purge signal." Accordingly, the Office Action fails to establish a *prima facie* case of obviousness with respect to at least the features of "logic configured to receive a purge signal and to make a determination as to whether any of the translation pairs stored in the TLB

correspond to the purge signal, the logic configured to purge from the TLB each translation pair corresponding to the purge signal, ***the logic further configured to determine, based on the determination, whether to purge the instruction queue in response to the purge signal***," as recited by claim 25. (Emphasis added).

For at least the above reasons, Applicants assert that the cited art fails to suggest each feature of claim 25. Accordingly, Applicants respectfully request that the 35 U.S.C. §103 rejection of claim 25 be withdrawn.

Claims 26 and 27

Claims 26 and 27 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over AAPA in view of *Moore*. Applicants submit that the pending dependent claims 26 and 27 contain all features of their respective independent claim 25. Since claim 25 should be allowed, as argued hereinabove, pending dependent claims 26 and 27 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 28

Claim 28 presently stands rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over AAPA in view of *Moore*. Claim 28 reads as follows:

> 28. A method, comprising the steps of:
> storing a plurality of translation pairs in a translation lookaside buffer (TLB), each of the translation pairs having a respective virtual address and a respective physical address;
> receiving a purge signal identifying at least one stale translation pair;
> ***determining whether any of the plurality of translation pairs in the TLB are identified by the purge signal***;
> if at least one of the plurality of translation pairs in the TLB is identified by the purge signal, purging the at least one translation pair identified by the purge signal; and
> ***determining whether to purge at least one component of a memory cache other than the TLB based on the step of determining whether any of the plurality of translation pairs in the TLB are identified by the purge signal.***" (Emphasis added).

For at least reasons similar to those set forth above in the arguments for allowance of claim 25, Applicants respectfully assert that the cited art fails to suggest at least the features of claim 28 highlighted above. Thus, the 35 U.S.C. §103 rejection of claim 28 should be withdrawn.

Claims 29-31

Claims 29-31 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over AAPA in view of *Moore*. Applicants submit that the pending dependent claims 29-31 contain all features of their respective independent claim 28. Since claim 28 should be allowed, as argued hereinabove, pending dependent claims 29-31 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

CONCLUSION

Applicants respectfully request that all outstanding objections and rejections be withdrawn and that this application and all presently pending claims be allowed to issue. If the Examiner has any questions or comments regarding Applicants' response, the Examiner is encouraged to telephone Applicants' undersigned counsel.

Respectfully submitted,

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